Networking Workloads on Intel Architecture

Communications, Storage and Infrastructure Group
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What does the Intel DPDK team do?

Implement new features/libraries to aid networking workloads
- Ongoing process as we discover bottlenecks/problems
- Customer feedback

Continuous performance improvement of existing libraries
- Pure code optimizations on existing platforms
- New/improved algorithmic implementations
- With multiple CPU architectures (Intel® Xeon®, Atom)

Recommend & drive enhancements
- To further packet processing solutions on Intel Architecture platforms

<table>
<thead>
<tr>
<th>Core Libraries</th>
<th>Platform</th>
<th>Packet Access (PMD – Native &amp; Virtual)</th>
<th>QoS User Space</th>
</tr>
</thead>
<tbody>
<tr>
<td>EAL</td>
<td>Packet F*WORK</td>
<td>ETHDEV</td>
<td>LPM</td>
</tr>
<tr>
<td>MALLOC</td>
<td>DISTRIB</td>
<td>E1000</td>
<td>EXACT MATCH</td>
</tr>
<tr>
<td>MBUF</td>
<td></td>
<td>I40e</td>
<td>ACL</td>
</tr>
<tr>
<td>MEMPOOL</td>
<td></td>
<td>VMXNET3</td>
<td>LPM</td>
</tr>
<tr>
<td>RING</td>
<td>KNI</td>
<td>VIRTIO</td>
<td>EXACT MATCH</td>
</tr>
<tr>
<td>TIMER</td>
<td>POWER</td>
<td>XENVIRT</td>
<td>ACL</td>
</tr>
<tr>
<td></td>
<td>IVSHMEM</td>
<td>PCAP</td>
<td>METER</td>
</tr>
</tbody>
</table>

Intel® DPDK Sample Applications

Customer Applications

ISV Eco-System Applications

2011 2012 2013 2014

Customer Applications

3rd Party NIC

QoS

User Space
The Challenge
## Intel® DPDK Performance

**A snapshot of on different architectures**

<table>
<thead>
<tr>
<th>Platform Features</th>
<th>Integrated Memory Controller PCI-E Gen2</th>
<th>Data Direct I/O Integrated PCI-E Gen3 AVX1 (integer)</th>
<th>4x10 GbE NICs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>System Level L3 Performance (MPPS)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2009</td>
<td>42</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2010</td>
<td>55</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2011</td>
<td>93</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2012</td>
<td>164.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2013</td>
<td></td>
<td>255</td>
<td></td>
</tr>
</tbody>
</table>

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Per core I/O performance ...

Performance of DPDK releases on E5-2680v2 (2.80 GHz)

Initial scalar fast-path with “auto-vectorization”, LIFO mempool

Original Rx & Tx path

94.5 cycles

29.6 mpps

r1.1
Apr '12

34.8 mpps

80.36 cycles

cache

r1.2
Oct '12

74.70 cycles

37.4 mpps

r1.3
Mar '13

59.12 mpps

Vector Rx & Tx (intrinsics)

r1.4
Jun '13

47.36 cycles

r1.5
Sep '13

47.36 cycles

r1.6
Feb '14

34.8 mpps

29.6 mpps

r1.7
Jul '14

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Changes under consideration ...

Improving performance further ...

• Patches to rework the original 1.1 “slow” path with a faster version
• Re-organized mbuf to carry more metadata from NIC
• Investigating implementation using AVX2
• Latency ...

Performance improvements to the exact match library (rte_hash)

• Faster hash functions
• Higher flow count (16M, 32M flows)
• Characterize/limit memory bandwidth usage
• Different algorithmic implementation – cuckoo hash
DPDK and latency ....

L3fwd default tuning is for performance

- Coalesces packets up to 100us
- Receives and transmits at least 32 packets at a time
  - \( \text{nb}_\text{rx} = \text{rte}_\text{eth}_\text{rx}_\text{burst}(\text{portid}, \text{queueid}, \text{pkts}_\text{burst}, \text{MAX}_\text{PKT}_\text{BURST}); \)

Could bunch 8, 4, 2, or even 1 packet(s) and trade-off some performance

- Lower coalescing increases transmit cost per packet
- Even at ~200 cycles per packet on a CPU running at > 2 GHz software isn’t a big adder to latency
Larger system-wide investigations

API versioning

Dynamic management of DPDK resources
  • CPU/Threads, memory, network

Sharing DPDK core with other pthreads
  • Adding interrupt-based entry, cgroups controlled time-sharing

Sharing NIC port between DPDK and kernel
  • VFIO, bifurcated driver
Building applications on top of DPDK

Packet distribution using NIC mechanisms (RSS, Flow Director etc.)

Run to completion

SW Pipeline

Core

NIC Rx

Packet Rx

Process

Packet Tx

NIC Tx

HW Queues

HW Queues

SW Queue (rte_ring)
Run-to-completion or Pipeline?

DPDK doesn't impose a model – both are supported, as are hybrid approaches

- Each has their advantages and disadvantages
- Have tools/benchmarks to evaluate either approach

Direction should be dictated by

- Legacy code & TTM considerations
- Performance requirements
- NIC limitations (e.g. RSS is purely IP packets only)
Assessing basic performance

app/test: Implements unit-tests and micro-benchmarks
- Micro-benchmarks exist for a number of libraries – labeled *_perf_autotest – mempool, hash, ring, timer, memcpy, distributor [adding nic in 1.8?]

app/testpmd: NIC I/O benchmark
- Benchmarks the network I/O pipe (NIC hardware + PMD)

elements/l3fwd: An example L3 forwarder
- Increased CPU processing – NIC hardware + PMD + hash/lpm

elements/load_balance: a simple load balancer in software

elements/ip_pipeline: Using the packet framework to build a pipeline

Intel uses these micro-benchmarks to drive performance
Summary

Multiple areas of improvement in the pipeline
  • Focus is on performance, functionality, usability

Looking for community input/participation
  • What are the problems that we need to solve?

Let’s discuss …
Backup
## The libraries/components (1)

<table>
<thead>
<tr>
<th>Library</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>librte_eal</td>
<td>Environment Abstraction Layer. Meant to hide system/OS specifics from “common” upper layers</td>
</tr>
<tr>
<td>librte_malloc</td>
<td>rte_malloc() - replacement for malloc(). Allows allocation of data structures backed by huge pages</td>
</tr>
<tr>
<td>librte_mempool</td>
<td>Memory management: DPDK buffer pool management and packet buffer implementations</td>
</tr>
<tr>
<td>librte_mbuf</td>
<td>记忆管理：DPDK缓冲池管理及数据结构实现</td>
</tr>
<tr>
<td>librte_ring</td>
<td>High speed ring for inter-core/process pointer passing</td>
</tr>
<tr>
<td>librte_timer</td>
<td>Timer routines</td>
</tr>
<tr>
<td>librte_lpm</td>
<td>Accelerated longest prefix match</td>
</tr>
<tr>
<td>librte_hash</td>
<td>Hash driven key-value exact match for tuple matching</td>
</tr>
<tr>
<td>librte_acl</td>
<td>Accelerated implementation of an Access Control List</td>
</tr>
</tbody>
</table>
## The libraries/components (2)

<table>
<thead>
<tr>
<th>Library</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>librte_meter</td>
<td>Meter/mark library: Implements srTCM (RFC 2697) and trTCM RFC 2698</td>
</tr>
<tr>
<td>librte_sched</td>
<td>Hierarchical traffic shaper in software</td>
</tr>
<tr>
<td>librte_pmd*</td>
<td>Packet Access “Poll” mode drivers</td>
</tr>
<tr>
<td>librte_ether</td>
<td>Generic Ethernet device abstraction – the DPDK PMD API</td>
</tr>
<tr>
<td>librte_cmdline</td>
<td>Command line parser library</td>
</tr>
<tr>
<td>librte_distributor</td>
<td>A work queue distributor</td>
</tr>
<tr>
<td>librte_power</td>
<td>Power management primitives</td>
</tr>
<tr>
<td>librte_ivshmem</td>
<td>Shared memory implementation for inter-VM communication</td>
</tr>
<tr>
<td>KNI, librte_kni</td>
<td>Kernel Network Interface – implements a kernel netdev for passing packets into the kernel from DPDK</td>
</tr>
</tbody>
</table>